Amendments to the Claims

1. (CURRENTLY AMENDED) A level shifter ~~(20)~~ comprising: a pair of current mirrors ~~(M1, M2; M3, M4)~~ that are configured to couple an input signal from a first system to a common output node (Vout) in a second system that is isolated from the first system, and a pair of diodes ~~(D1, D2)~~ that are configured to decouple one of the pair of current mirrors ~~(M1, M2; M3, M4)~~ from the input signal if a fault occurs.

2. (CURRENTLY AMENDED) The level shifter ~~(20)~~ of claim 1, wherein the pair of current mirrors ~~(M1, M2; M3, M4)~~ comprise transistors ~~(M1-M4)~~ that are each of the same channel-type.

3. (CURRENTLY AMENDED) The level shifter ~~(20)~~ of claim 1, wherein the pair of diodes ~~(D1, D2)~~ are further configured to split current ~~(Iin1, Iin2)~~ from the input signal ~~(Iin)~~ to provide substantially half the current to each of the pair of current mirrors ~~(M1, M2; M3, M4)~~ when the fault does not occur.

4. (CURRENTLY AMENDED) The level shifter ~~(20)~~ of claim 1, wherein a first current mirror ~~(M1, M2)~~ of the pair of current mirrors ~~(M1, M2; M3, M4)~~ is supplied by a first reference voltage ~~(Vdd1)~~ of the first system, and a second current mirror ~~(M3, M4)~~ of the pair of current mirrors ~~(M1, M2; M3, M4)~~ is supplied by a second reference voltage ~~(Vdd2)~~ of the second system.

5. (CURRENTLY AMENDED) The level shifter ~~(20)~~ of claim 4, further comprising a third diode (D3) that is configured to decouple the first current mirror ~~(M1, M2)~~ from the common output node ~~(Vout)~~ if the fault occurs.

6. (CURRENTLY AMENDED) The level shifter ~~(20)~~ of claim 1, further including a current generator ~~(Icomp)~~ that is configured to provide a compensation current between the first system and the second system, to minimize a net current flow between the first system and the second system.

7. (CURRENTLY AMENDED) The level shifter ~~(20)~~ of claim 1, further including a voltage source ~~(Vos)~~ that is configured to provide bias between the first system and the second system to minimize switching transients.

8. (CURRENTLY AMENDED) A level shifter ~~(30-170)~~ for coupling an input signal ~~(Iin, Vin)~~ from a first system to an output node ~~(Vout)~~ in a second system that is isolated from the first system, comprising: a current mirror ~~(M1, M2)~~ that is

configured to mirror current corresponding to the input signal ~~(Iin, Vin)~~ to a load at the output node ~~(Vout)~~, and a pair of diodes ~~(D1, D2)~~ that is configured to select a reference voltage ~~(Vmax, Vmin)~~ from one of the first system and the second system to provide a net current to the current mirror ~~(M1, M2)~~.

9. (CURRENTLY AMENDED) The level shifter ~~(40)~~ of claim 8, further including: at least one other current mirror ~~(M3, M4; M3, M5)~~ that is configured to mirror the current corresponding to the input signal ~~(Iin, Vin)~~ to at least one other load ~~(L2b)~~ in at least one other system, and at least one other diode ~~(D3)~~, operably coupled to the pair of diodes ~~(D1, D2)~~ to form a diode network that is configured to select the reference voltage ~~(Vmax, Vmin)~~ from one of the first system, the second system, and the at least one other system, to provide the net current to the current mirror.

10. (CURRENTLY AMENDED) The level shifter ~~(40)~~ of claim 8, further including: a second current mirror ~~(M6, M7)~~ that is configured to mirror another current corresponding to an input ~~(Iin3)~~ from the second system to an other load ~~(L3)~~ in the first system.

11. (CURRENTLY AMENDED) The level shifter ~~(30a)~~ of claim 8, wherein the current mirror ~~(M1, M2)~~ comprises P-channel transistors, a first diode ~~(D1)~~ of the pair of diodes ~~(D1, D2)~~ is arranged in series between a first supply voltage (Vdd1) of the first system and the current mirror ~~(M1, M2)~~, and a second diode ~~(D2)~~ of the pair of diodes ~~(D1, D2)~~ is arranged in series between a second supply voltage ~~(Vdd2)~~ of the second system and the current mirror ~~(M1, M2)~~, so that the reference voltage ~~(Vmax)~~ corresponds to whichever of the first supply voltage ~~(Vdd1)~~ and the second supply voltage ~~(Vdd2)~~ is at a higher potential.

12. (CURRENTLY AMENDED) The level shifter ~~(30b)~~ of claim 8, wherein the current mirror ~~(M1, M2)~~ comprises N-channel transistors, a first diode ~~(D1)~~ of the pair of diodes ~~(D1, D2)~~ is arranged in series between the current mirror and a first ground voltage ~~(Vgnd1)~~ of the first system, and a second diode ~~(D2)~~ of the pair of diodes ~~(D1, D2)~~ is arranged in series between the current mirror and a second ground voltage ~~(Vgnd2)~~ of the second system, so that the reference voltage ~~(Vmin)~~ corresponds to whichever of the first ground voltage ~~(Vgnd1)~~ and the second ground voltage ~~(Vgnd2)~~ is at a lower potential.

13. (CURRENTLY AMENDED) The level shifter ~~(60)~~ of claim 8, further including a second current mirror ~~(M7, M9; M8, M10)~~ that is configured to mirror a second current corresponding to an inversion of the input signal ~~(Vin)~~ to provide a differential output ~~(M10, M12)~~ in the second reference system.

14. (CURRENTLY AMENDED) The level shifter ~~(60)~~ of claim 8, further including one or more bias transistors ~~(M30-M33)~~ that is configured to provide a bias current to the current mirror to enhance a switching speed of the current mirror.

15. (CURRENTLY AMENDED) The level shifter ~~(50)~~ of claim 8, further including cascode transistors ~~(M11-M16;)~~ corresponding to each transistor in the current mirror ~~(M1-M6)~~.

16. (CURRENTLY AMENDED) The level shifter ~~(50)~~ of claim 15, further including one or more current-injecting transistors ~~(M22, M26)~~ that is configured to reduce the effects of gate-drain capacitance associated with one or more of the cascode transistors ~~(M11-M16)~~.

17. (CURRENTLY AMENDED) The level shifter ~~(50)~~ of claim 15, further including one or more isolation transistors ~~(M25)~~ that is configured to decouple the effects of gate-drain capacitance associated with one or more of the cascode transistors ~~(M11-M16)~~ from the input signal ~~(Iin, Vin)~~.

18. (CURRENTLY AMENDED) The level shifter ~~(70-140, 160-170)~~ of claim 8, further including a current generator ~~(Icomp)~~ that is configured to provide a compensation current between the first system and the second system, to substantially minimize a net current flow between the first system and the second system.

19. (CURRENTLY AMENDED) A method of coupling an input signal ~~(Iin, Vin)~~ from a first system to a common output node ~~(Vout)~~ in a second system that is isolated from the first system, comprising: coupling the input signal ~~(Iin, Vin)~~ to the common output node via a pair of current mirrors ~~(M1, M2; M3, M4)~~, and providing a pair of diodes ~~(D1, D2)~~ that are configured to decouple one of the pair of current mirrors ~~(M1, M2; M3, M4)~~ from the input signal ~~(Iin, Vin)~~ if a fault occurs.

20. (CURRENTLY AMENDED) A method of coupling an input signal ~~(Iin, Vin)~~ from a first system to a common output node ~~(Vout)~~ in a second system that is isolated from the first system, comprising: mirroring current corresponding to the input signal ~~(Iin, Vin)~~ to a load at the output node ~~(Vout)~~ via a current mirror ~~(M1, M2)~~,

and selecting a reference voltage ~~(Vmax, Vmin)~~ from one of the first system and the second system via a pair of diodes ~~(D1, D2)~~, to provide a net current to the current mirror ~~(M1, M2)~~.